

Appl. No. 10/615,918
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Appendix 1

CLEAN FORMAL DRAWING SHEET
AMENDED FIGURE 7

Stall for Next to Last PipeStage (NLP)

Stall (NLP) = Valid Instruction in Pipe (NLP) AND ThreadId (NLP) = ThreadId of Stall)

Stall for any other PipeStageX

Stall(X) = Valid Instruction in Pipe(X) AND Valid Instruction in Pipe(X+1) AND Stall (NLP)

Powerdown for any PipeStage X

Powerdown(X) = NOT Valid Instruction in Pipe(X-1)

Clock Enable for any PipeStage X

Clock(X) = NOT Stall(X) AND NOT Powerdown(X)

Clear for any PipeStage X

Clear(X) = Clock(X) AND [(ClearThread(Id0) AND (ThreadId(X-1) = Id0)) OR (ClearThread (Id1) AND (ThreadId (X-1) = Id1))]
OR
NOT Clock(X) AND [(ClearThread(Id0) AND (ThreadId(X) = Id0)) OR (ClearThread(Id1) AND (ThreadId(X) = Id1))]

ClearThread (Id0) = There was a Clear on Thread Identification 0

ClearThread (Id1) = There was a Clear on Thread Identification 1

Pipe(X) = Any pipestage in the decode

Pipe(X-1) = Pipestage before Pipe(X)

Pipe(X+1) = Pipestage after Pipe(X)

FIG. 7